Subranging BJT-Based CMOS Temperature Sensor With a ±0.45 °C Inaccuracy (3σ) From −50 °C to 180 °C and a Resolution-FoM of 7.2 pJ·K^2 at 150 °C

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***Abstract*— This article presents a BJT-based CMOS temperature sensor with a wide sensing range from −50 °C to 180 °C. To effectively relax the sensor resolution requirement and conversion time over the entire temperature range to improve energy efficiency, we introduce a nonlinear subranging readout scheme together with double sampling to achieve dynamic reconfiguration of the sensor readout according to the ambient temperature. We further reduce the sensor power at high temperature by devoting the β-cancellation circuit only for BJT biasing while applying a temperature-independent bias current for the other sensor building blocks. Implemented in 0.18-μm CMOS with four-wire connections and switch-leakage compensation based on small BJTs, the proposed sensor chip prototype achieves a high resolution-FoM of 7.2 pJ·K^2 at 150 °C, while featuring a small sensing error of ±0.45 °C under a 1.5-V supply.**

***Index Terms*— BJT, calibration, double-sampling ADC, low-leakage switch, subranging readout, temperature sensor.**

I. Introduction

TEMPERATURE sensor for industrial applications such as electrical grid, turbine, and automotive must operate reliably over a wide temperature range (e.g., −40 °C to 150 °C [1]). In such harsh environments, discrete sensors like thermocouples or thermistors were traditionally employed for their robustness and well-defined response. However, their high power consumption for signal acquisition, large form factor, and process incompatibility with the interface electronics limit their applications in modern smart sensing systems, which are often power-, energy-, and size-constrained [2], [3].

Among the CMOS integrated temperature sensors [4], resistor-based ones utilizing the temperature coefficient (TC) of resistors become increasingly popular as they can achieve superior sub-pJ·K^2 resolution-FoM [5] as well as high accuracy after one-point trim with polynomial curve fitting [6]. The recent self-calibration approach assisted by a thermal-diffusivity sensor further reduces the calibration cost [7]. However, resistor-based temperature sensors are highly dependent on the temperature dependency of on-chip resistors and may not be favorable in processes with only small TC resistors [8]. In contrast, owing to the stable thermal characteristics and good reproducibility of BJTs [9], BJT-based temperature sensors can satisfy the above design constraints and achieve good performance at high temperature (high-T) with one-point trim, simple digital processing, and good process scalability [10], [11], [12], [13].

For BJT-based sensors designed in bulk CMOS, the device nonlinearity and leakage can be the major performance killers at high-T and are traditionally addressed by using a larger bias current [10], or employing leakage reduction techniques [14], [15]. However, prior designs primarily focused on the sensor performance at room temperature (RT) [16]. Yet, their power consumption could increase rapidly to compensate for the increased noise and leakage current at high-T. This can severely degrade the overall energy efficiency and hinder their deployment in practical harsh environment scenarios [2].

This article presents a BJT-based temperature sensor targeting for a wide sensing range from −50 °C to 180 °C (expanded from [17]). The proposed subranging double-sampled readout scheme reconfigures the sensor dynamically according to the ambient temperature. This can reduce both the required sensor readout resolution and temperature conversion time, thus improving the sensor energy efficiency. Meanwhile, this design only devotes the β-cancellation circuit for BJT biasing while employing a reference current to bias the other sensor building blocks. Such an arrangement, together with clock-gated digital circuits using high-V_{th} devices, can avoid sharp sensor power increase at high-T. The leakage-compensated sampling switches can also ensure accurate sensing at high-T without increasing the frontend power consumption.

This article is organized as follows. Section II presents the system-level sensor optimization. The sensor implementation and operation are presented in Section III. Section IV elaborates on the experimental results. Section V concludes.

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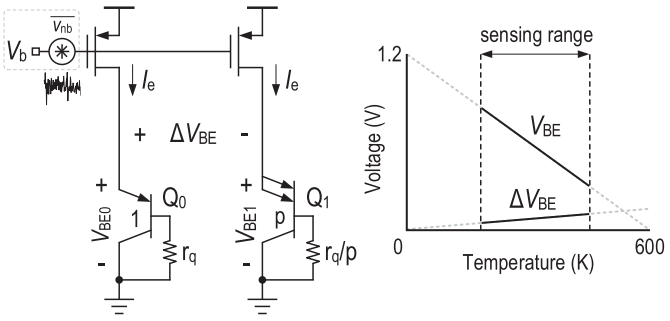


Fig. 1. PNP core to generate the sensing signals V_{BE} and ΔV_{BE}.

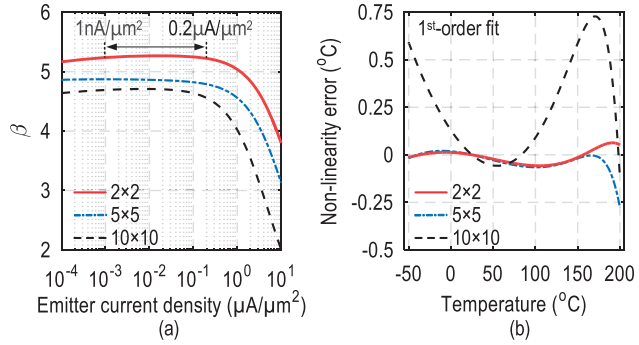


Fig. 2. For PNPs with different emitter areas. (a) Simulated β with respect to emitter bias current density at 180 °C. (b) Sensing error due to nonlinearity in V_{BE} and ΔV_{BE}, with $p = 8$ and a PTAT bias I_e (150 nA at 25 °C).

II. Optimization of BJT-Based Temperature Sensor for Wide-Range Operation

A. BJT and BJT Biasing

Identifying and minimizing error sources from BJTs are essential to ensure good sensing accuracy over a wide operating range. Fig. 1 shows the sensor core for generating the temperature-dependent signals V_{BE} (i.e., V_{BE0}) and ΔV_{BE} (i.e., $V_{BE0} - V_{BE1}$) [9]. For low-power operation, the two pnp BJTs, Q_0 and Q_1, carry the same emitter bias I_e, while having an emitter area ratio of $1 : p$. Therefore,

$$V_{BE} \approx \eta \cdot V_T \cdot \ln\left(\frac{I_e}{I_s} \cdot \frac{\beta}{\beta+1} + 1\right) + r_q \cdot \frac{I_e}{\beta+1} \tag{1}$$

and

$$\Delta V_{BE} \approx \eta \cdot V_T \cdot \left[\ln(p) + \ln\frac{I_e + I_s(1+1/\beta)}{I_e + p \cdot I_s(1+1/\beta)}\right] + r_q \cdot \frac{I_e}{\beta+1} \cdot \frac{p-1}{p} \tag{2}$$

where V_T is the thermal voltage, η is the BJT's nonideality factor, I_s is its saturation current, β is its nominal forward current gain, and r_q is its terminal resistance referred to the base. In (2), we assumed both Q_0 and Q_1 exhibit the same β through selecting an appropriate I_e [18]. The temperature sensitivities of V_{BE} and ΔV_{BE} are near-constant if $I_e \gg I_s$ holds [10]. However, this condition weakens at high-T due to the exponential increase of I_s, leading to substantial nonlinearities in V_{BE} and ΔV_{BE}. As indicated by (1) and (2), except for ensuring $I_e \gg I_s$, adopting a pnp BJT with a small I_s, a large β, and a small p can help to minimize the nonlinearity terms.

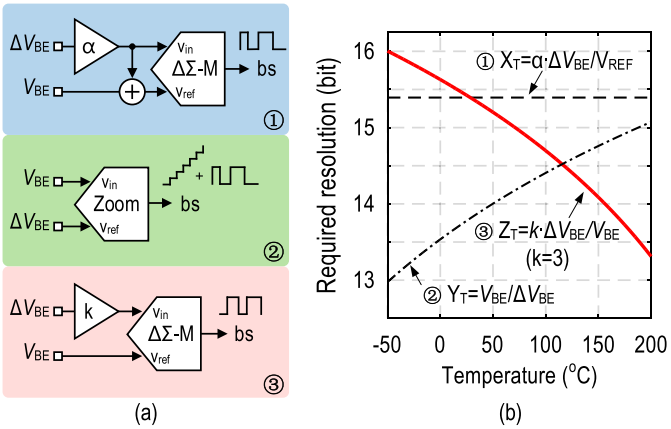


Fig. 3. (a) Illustration of different readout schemes. (b) Readout resolution requirement[1] to achieve a sensing resolution of 15 m°C. The simulation setup is the same as Fig. 2(b) using a 2 μm × 2 μm BJT.

Based on the simulation results in Fig. 2(a), this work employs a pnp BJT with a small emitter area of 2 μm × 2 μm, which enjoys a relatively larger β under the same bias current densities at high-T. An emitter bias current density from 1 to 200 nA/μm^2 can result in a negligible current dependence in β. Meanwhile, we adopted $p = 8$ considering the tradeoff between the temperature sensitivity and linearity of ΔV_{BE}. Under these design constraints, the sensing error introduced by r_q, which is around 100 Ω as specified in the device model, becomes negligible. As shown in Fig. 2(b), the overall sensing error of the adopted BJT due to signal nonlinearity is about 0.05 °C from −50 °C to 180 °C after a first-order fit.

B. Sensor Readout Selection

There are different methods to combine V_{BE} and ΔV_{BE} to produce a digital representation of temperature, as depicted in Fig. 3(a). The classical way is to digitize the ratio $X_T = \alpha \cdot \Delta V_{BE}/V_{REF}$, where α is a constant to produce an on-chip indirect reference voltage $V_{REF} = \alpha \cdot \Delta V_{BE} + V_{BE}$ [19]. This scheme is not flexible since the gain α, as determined by the process model, is typically built-in within the sensor readout. It also amplifies the noise power in ΔV_{BE} by α^2 during sampling. Another popular scheme is to digitize the ratio $Y_T = V_{BE}/\Delta V_{BE}$ with a two-step zoom ADC [20], whose output is a nonlinear function of temperature but can be handily linearized in the digital backend. However, this scheme should sample V_{BE} in every clock cycle. Since ΔV_{BE} is small and often amplified during readout, its noise contribution is usually dominant. However, the noise contribution of V_{BE} may be significant in low-power designs, as discussed below.

As shown in Fig. 1, the noise $\overline{v_{nb}}$ associated with the BJT core bias V_b (also see Fig. 10) appears in $V_{BE0,1}$ as a common mode noise, which can be suppressed during ΔV_{BE} sampling but not when sampling V_{BE}. Depending on the bias generator design, the noise added to V_{BE} via V_b could be significant as indicated in Fig. 4, which shows the simulated noise profile of V_{BE} and ΔV_{BE} of the designed sensor frontend at RT (details in Section III-B). Although the noise contribution from V_{BE} and ΔV_{BE} to the digitized output also depends on the readout

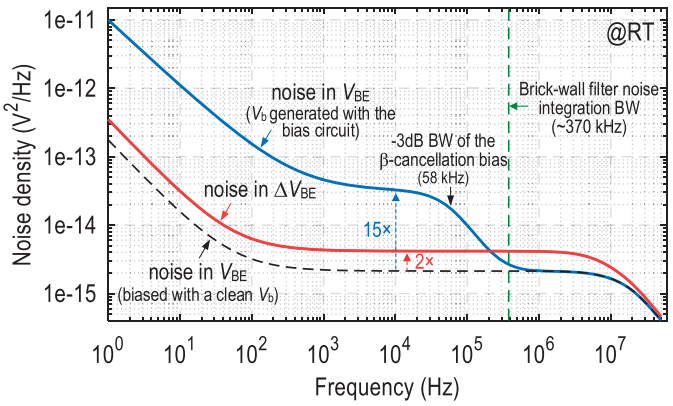


Fig. 4. Simulated noise power density in V_{BE} and ΔV_{BE} with and without including the noise source $\overline{v_{nb}}$ (frontend design details in Section III-B).

configuration, especially the ΔV_{BE} gain (e.g., α in [19]), it is still beneficial if we can minimize the number of V_{BE} sampling in one temperature conversion to reduce the total noise sampled from the sensor frontend, especially for low-power high-resolution sensors. With this consideration, this work digitizes the ratio $Z_T = k \cdot \Delta V_{BE}/V_{BE}$ as it does not sample V_{BE} in every clock cycle, with k being a gain factor to accommodate for the readout dynamic range [11], [21]. k (set to be 3 or 6 in this work) is smaller than α (=16) in [19] or $\lfloor V_{BE}/\Delta V_{BE} \rfloor_{max}$ (=28) in the zoom ADC readout [20].

Considering from another perspective, these readouts have different requirements to achieve the same sensing resolution. As shown in Fig. 3(b), to achieve a target resolution of 15 m°C over a wide temperature range, compared to other schemes, digitizing Z_T offers a gradually relaxed readout resolution requirement[1] at high-T when the system becomes noisier. This feature is preferred in our design, which aims to optimize the sensor performance at high-T. After conversion, we can linearize Z_T by

$$\mu_T = \alpha/(\alpha + k/Z_T). \tag{3}$$

With a first-order fit of μ_T, the digital representation (in °C) of the measured temperature is

$$D_{out} = A \cdot \mu_T + B \tag{4}$$

where $A \approx 600$ and $B \approx -273$ are constants, with their exact values derived via batch calibration. A higher-order fit of μ_T can be applied when systematic nonlinearity exists [16].

C. Subranging Scheme

The main issue for digitizing Z_T is its high readout resolution requirement at low temperatures (low-T) as observed in Fig. 3(b). By designing the sensor for the worst case, that is, 16-bit at −50 °C referenced V_{BE}, the sensor can waste an excessively large power at high-T as only 13.5-bit is necessary for resolving the target temperature resolution at 180 °C.

[1]Required resolution for digitizing Z_T is $\log_2[(\partial\mu_T/\partial Z_T)/(\partial\mu_T/\partial T)/R]$ under the condition of $k\Delta V_{BE} \leqslant V_{BE}$, where R is the target sensing resolution. See [9] and [22] for the required resolution of digitizing X_T and Y_T, respectively.

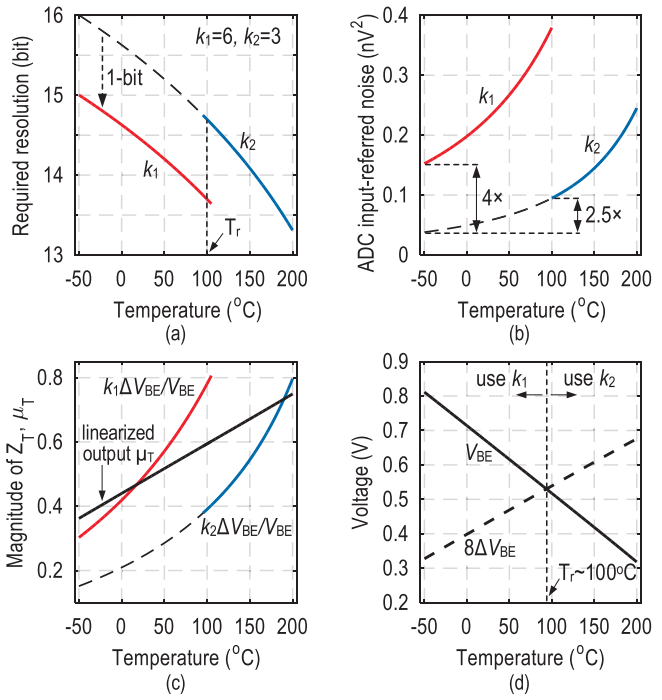


Fig. 5. (a) Subranging scheme. (b) Total ADC input-referred[2] noise requirement (including quantization noise, thermal noise from the ADC, and thermal noise from the frontend). (c) Magnitudes of Z_T, μ_T. (d) Subranging decision.

In this work, we employ a subranging scheme to achieve a high energy efficiency over the entire temperature range. As illustrated in Fig. 5(a), for temperatures below the transition temperature $T_r \sim 100$ °C, that is, the low-T subrange, we set the signal gain for ΔV_{BE} to 6 (i.e., k_1) to relax the system resolution requirement by 1 bit. For temperatures above T_r, that is, the high-T subrange, the corresponding gain for ΔV_{BE} is set to 3 (i.e., k_2) to avoid overloading the readout. As observed in Fig. 5(b), this can relax the total ADC input-referred[2] noise power requirement by 4× and 2.5× for the two subranges, respectively. Note that changing the gain k does not affect the temperature reading after linearization. Fig. 5(c) shows the simulated magnitude of Z_T and μ_T. With the selected $k_{1,2}$ and T_r, we can maintain Z_T to be less than 0.8 for ensuring the stability of a second-order incremental ADC [23].

As presented in Fig. 5(d), the subrange control is achieved by checking the polarity of $(8\Delta V_{BE} - V_{BE})$ before each conversion. For temperatures near the transition temperature, either k_1 or k_2 can be employed, thus noise and process induced variations of T_r are highly tolerable. Applying more subranges is possible at the cost of increased control complexity.

D. Faster Conversion

For a low-power BJT-based temperature sensor, irrespective of the readout details, its frontend power is often determined by the bias generator's settling requirement (e.g., for dynamic error correction) and its BJT core biasing (e.g., usually larger than the current required for settling during $V_{BE0,1}$ sampling) [9]. Therefore, for a given readout sampling frequency

[2]The node after the gain k in the ideal model of Fig. 3(a).

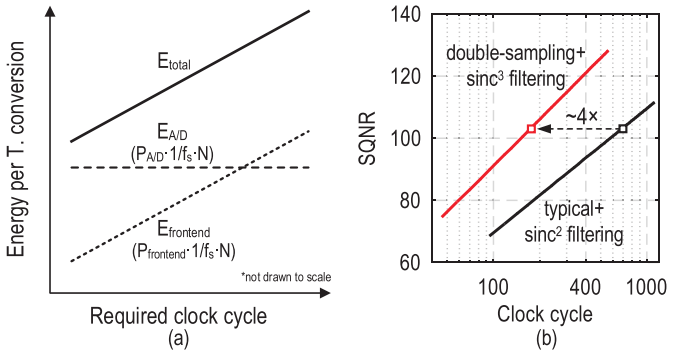


Fig. 6. (a) Illustration of the sensor energy consumption per conversion E_{total} with the required conversion clock cycles (for a given readout sampling frequency f_s and resolution target). (b) SQNR versus clock cycles for a second-order modulator.

f_s (e.g., 40 kHz in this design), energy consumed by the sensor frontend E_{frontend} scales linearly with the number of clock cycles N in one temperature conversion, as illustrated in Fig. 6(a). In contrast, to achieve a target thermal-noise-limited resolution (e.g., 15-bit), energy consumed by the readout $E_{\text{A/D}}$ is nearly constant irrespective of N. This is because if N increases, the modulator's sampling capacitance, thus its power consumption will decrease proportionally (thermal noise averaging cycle $\propto N$) [23].

Depending on the design choices, the power consumed by the sensor frontend can take up 30% [21], 57% [11], or even more than 70% [18] of the sensor's total power. Therefore, for a given f_s and resolution target, it is beneficial if N can be minimized. In addition, the sensor's digital power could be significant at high-T (e.g., consuming 36% of the sensor's total power at 180 °C in our design); a smaller N can also reduce its energy consumed per temperature conversion.

In this work, we employ double-sampling to achieve a faster conversion. By sampling the input and feedback signals in both ϕ_1 and ϕ_2, and with the quantizer evaluating twice per clock cycle, the number of clock cycles required for one temperature conversion can be halved without burning extra power or sacrificing the effective thermal noise averaging cycle [24], [25]. Meanwhile, we adopt a second-order modulator with a sinc^3 instead of the often adopted sinc^2 filter for output decimation [26]. It can reduce the required conversion cycle by $\sim$2×, thus halving the energy consumed by the sensor frontend and digital controller. Because the sinc^3 filter has a higher thermal noise penalty ($\sim$1.6 compared with $\sim$1.3 of sinc^2 [27]) and N is halved, compared to that of using a sinc^2, the readout sampling capacitance should be increased correspondingly (e.g., by $\sim$2.4× in this work). Yet, the energy savings from the sensor frontend and digital controller due to a $\sim$2× faster conversion can lead to a significant overall energy reduction (e.g., about 30 nJ per temperature conversion using sinc^3 in this work, compared to 48 nJ using sinc^2). This is especially true for low-power designs where the frontend and digital controller contribute to a significant portion of the overall sensor power consumption (e.g., [18]).

As shown in Fig. 5(a), the required system resolution is 15-bit after employing subranging. With the above readout arrangement, running the modulator for 160 clock cycles can handily suppress its quantization noise power to a negligible level (i.e., 102 dB SQNR, 10× below the target noise level), as depicted in Fig. 6(b). It is one-fourth of the cycles required by a typical modulator that only samples the input/feedback signal and operates the quantizer once per clock cycle.

E. One-Point Calibration

For BJT-based designs, one-point trim is typically necessary to correct the spread of V_{BE} [9], and the trimmed output can be expressed as

$$\mu_{T\_\text{cal}} = \alpha/(\alpha + \Delta\alpha + k/Z_{T\_\text{out}}) \tag{5}$$

where $Z_{T\_\text{out}} = k \cdot (1 + \sigma_k) \cdot \Delta V_{\text{BE}}/V_{\text{BE}}$ is the actual sensor output to be calibrated, with σ_k representing the spread of k. $\Delta\alpha$ is the sensor's trimming coefficient such that its trimmed output equals to the desired μ_{T0} at the calibration temperature T_0 (e.g., RT, use k_1), with

$$\Delta\alpha = \alpha/\mu_{T0} - \alpha - k_1/Z_{T0\_\text{out}}. \tag{6}$$

Unlike the V_{BE} spread, σ_k cannot be corrected by $\Delta\alpha$. To resolve this issue, [11] employed only one sampling capacitor with multiple integration cycles to achieve an accurate gain, but at the cost of reduced energy efficiency. To limit the sensing error caused by σ_k to be below 0.1 °C, σ_k should be within 0.05%. In our design, this gain accuracy is achievable with the adopted large sampling capacitor size (a few pF), together with local capacitance averaging and common-centroid layout. When needed, we can perform a second RT trim by applying known input voltages to the readout for deriving the actual gain ($= Z_{T0\_\text{out}} \cdot V_{\text{ref}}/V_{\text{in}}$) to correct σ_k.

On the other hand, if k_1/k_2 deviates from the designed ratio (i.e., 2 in this work), applying the ideal k_1 and k_2 (i.e., 6 and 3) to (5) for the low-T and high-T subrange calibration, respectively, would cause a discontinuity in μ_{T_cal} between the two subranges at T_r. In other words, it will introduce a step temperature change at T_r (e.g., about 0.15 °C with a 0.1% k_1/k_2 ratio error). To address this issue, we perform one extra correction step by converting the same temperature (i.e., RT) twice with different gain settings ($k_{1,2}$). We can then extract the actual gain ratio $k_1/k_2 = Z_{T0\_k1}/Z_{T0\_k2}$ to be applied for the high-T subrange calibration, expressed as

$$\mu_{T\_\text{cal\_high-T}} = \alpha/\left(\alpha + \Delta\alpha + Z_{T0\_k2}/Z_{T0\_k1} \cdot k_1/Z_{T\_\text{out}}\right). \tag{7}$$

Therefore, even with subranging, we can still perform sensor calibration at RT with a comparable calibration cost to the existing BJT-based designs.

III. Implementation

The proposed sensor is shown in Fig. 7, which consists of a sensor frontend, a switched capacitor (SC) $\Delta\Sigma$-ADC readout, a current reference generator, and a controller. We introduce the design considerations of the main building blocks as follows.

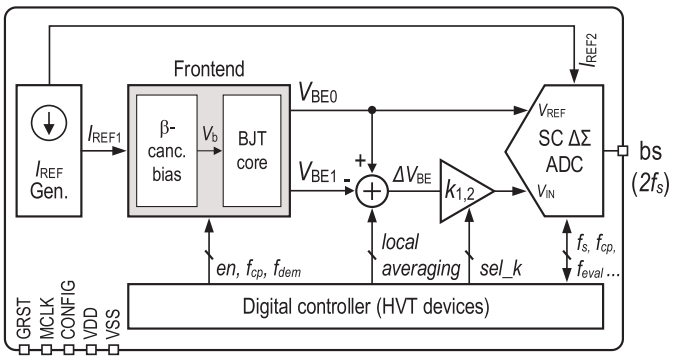


Fig. 7. Proposed subranging temperature sensor.

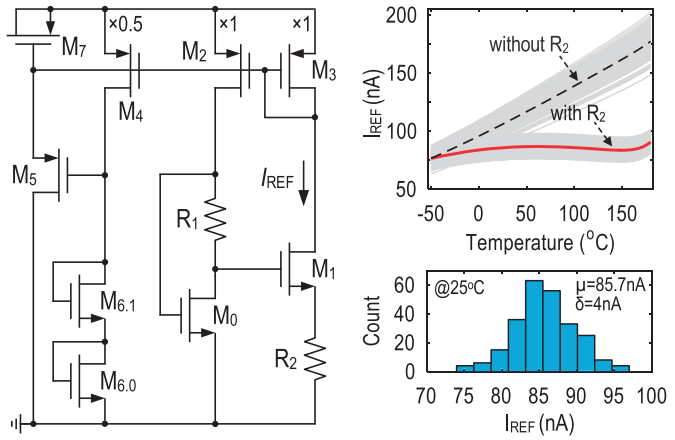


Fig. 8. (Left) I_{REF} generator (additional current mirrors not shown, M_0/M_1 aspect ratio is 1:2), and (right) the simulation results.

A. Sensor Current Reduction at High-T

In this design, instead of using a proportional-to-absolute-temperature (PTAT) current that can double the sensor's power consumption from −50 °C to 180 °C, we only use PTAT biasing for the BJT core, while employing a temperature-compensated reference current I_{REF} in Fig. 8 to bias the rest of the building blocks. Similar to [28], we utilize the TC of resistor (TCR) to minimize the temperature dependency of I_{REF} (∼86 nA at RT). The resistor R_1 of 65 kΩ is implemented using p-poly resistor with an averaged negative TCR of −780 ppm/°C, and R_2 of 220 kΩ being an n-well resistor with an averaged positive TCR of 3860 ppm/°C.

In addition, we implement all digital circuits with high-V_{th} transistors to minimize the channel leakage current at high-T. As illustrated in Fig. 9, at 180 °C, the static leakage of an inverter and a C^{2}MOS DFF [29] using high-V_{th} devices are 18 and 7 times less than that of using standard-V_{th} devices with the same transistor sizes, respectively. An even larger leakage can be observed for static DFFs in standard-V_{th} devices (i.e., around 50 nA at 180 °C). Therefore, besides clock-gating, digital design with a high-V_{th} device as performed in this design is crucial to reduce the sensor current at high-T.

B. Sensor Frontend

Fig. 10 shows the sensor frontend employing the classical β-cancellation biasing scheme [18], with $R_b = R_\beta$ (620 kΩ) to generate an I_e of 150 nA at RT. The biasing (0 V) of the

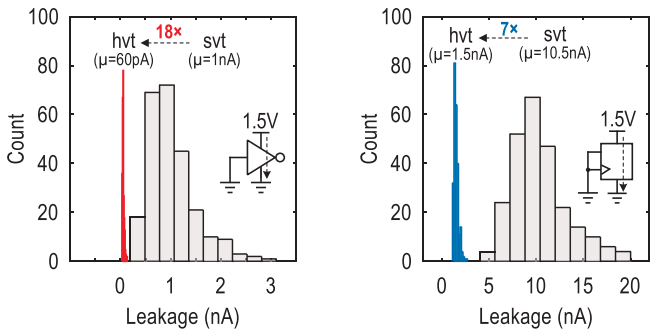


Fig. 9. Simulated leakage current of an inverter (pmos 0.22/0.3, nmos 0.22/0.35, in μm), and a CMOS master–slave DFF with asynchronous reset (pmos 0.6/0.3, nmos 0.42/0.35) using high-V_{th} devices (V_{th} at RT: nmos 0.66 V, pmos −0.73 V) and standard-V_{th} devices at 180 °C.

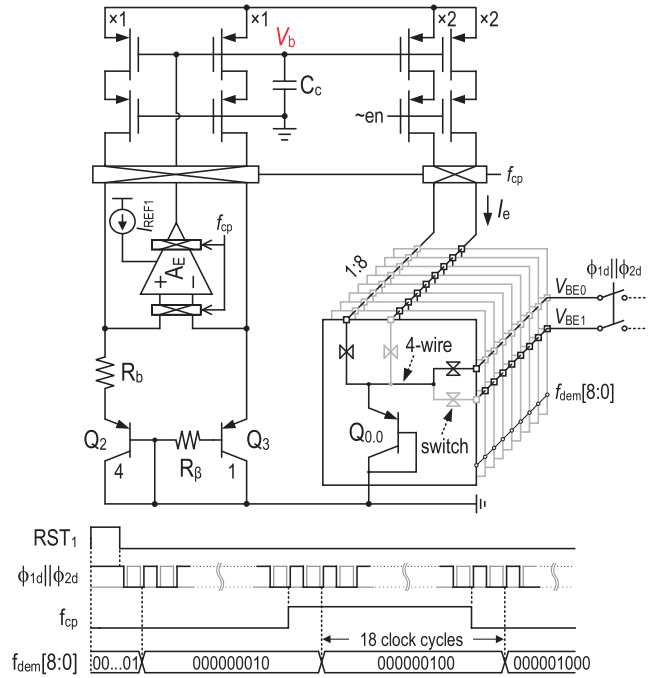


Fig. 10. Simplified sensor frontend and timing diagram (see the control signals RST_1 and $\phi_{1d,2d}$ in Fig. 14).

cascode PMOS in the current mirror can ensure low-voltage operation, but at the expense of a degraded negative supply rail rejection at high frequency. The 94-dB dc-gain folded-cascode error amplifier A_E consumes 0.45 μA, with its low-frequency noise being upmodulated by chopping. Mismatch of the current mirrors and BJT pair are mitigated by dynamic element matching (DEM) [13]. Four-wire connections at the BJT outputs can prevent accuracy degradation in $V_{BE0,1}$ due to the varying voltage drop across the DEM switches.

To reduce the noise bandwidth and power consumption of the β-cancellation bias circuit, its closed-loop −3 dB bandwidth is designed to be 58 kHz at RT. As the readout samples $V_{BE0,1}$ at $f_s = 40$ kHz, the settling of V_b, thus $V_{BE0,1}$, are slightly incomplete after each switch operation in the bias. In this design, we apply a relatively slow $f_{cp} = f_s/36$, which is above the simulated flicker noise corner frequency of the bias circuit over the target temperature range. Therefore, the settling error in V_b appears once every 18 clock cycles and becomes negligible after averaging. For example, the sensing

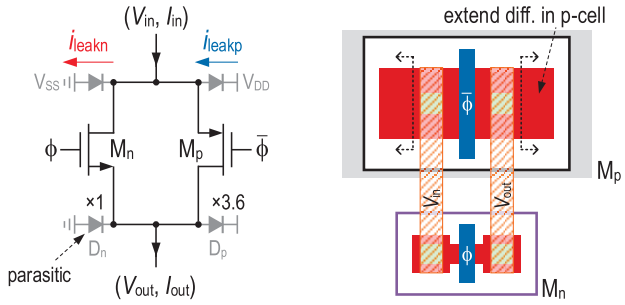


Fig. 11. Switch body-leakage compensation, and its layout with NMOS and PMOS size (in μm) being 0.22/0.18 and 0.8/0.18 in this design.

error due to this incomplete settling is only 4 m°C given a large offset of 20 mV in A_E.

The BJT DEM also runs at $f_s/36$ (via f_{dem}[8:0]), with its switching scheduled one cycle after chopping to minimize the transient voltage spikes in $V_{BE0,1}$, as illustrated in Fig. 10. Chopping and DEM are performed within the nonoverlapping region of the two sampling clock phases to maintain the fidelity of $V_{BE0,1}$ during sampling. Note that the intermodulation between the chopping and DEM residues with the bitstream via the feedback DAC can cause quantization noise folding, thus degrading the sensor resolution [19]. In this design, since we employed a slow chopping and DEM with minimized $V_{BE0,1}$ transient spikes, a simple fixed frequency chopping and DEM scheme is adopted.

C. Switch Body-Leakage Compensation

Regarding the switches employed for dynamic error corrections in the frontend, their maximum input and output voltage difference is ΔV_{BE}, which is less than 100 mV. Therefore, their OFF-state channel leakages are negligible, and simple transmission gates (TGs) are sufficient [14]. However, the body leakage of a transistor increases exponentially with temperature, effectively introducing nonlinearity to $V_{BE0,1}$ at high-T. As depicted in Fig. 11, the body-leakage current of NMOS and PMOS flow in the opposite direction in a TG. Based on the adopted process model, the diffusion area of PMOS is designed to be 3.6 times that of the NMOS to achieve a first-order body-leakage compensation.

For the extensively employed analog multiplexer for DEM in Fig. 12(a), the transistor source/drain diffusions are shared to further reduce the leakage current I_{leak} at the output node. Based on the measurement results in Fig. 12(b), I_{leak} is a few pA at 120 °C, reaches 630 pA at 180 °C, and can be reduced to 180 pA with body-leakage compensation. This can suppress the switch leakage-induced nonlinearity error in the frontend to be less than 0.1 °C. We can expect an even lower leakage by further fine-tuning (slightly increasing) the PMOS diffusion area. The effectiveness of this compensation scheme varies with the diffusion doping concentrations, which typically exhibits a process spread of ±15% in modern processes [9].

D. Double-Sampled Readout With Subrange Decision

1) Description: The sensor readout employs a 1-bit double-sampled second-order feed-forward SC ΔΣ-ADC considering

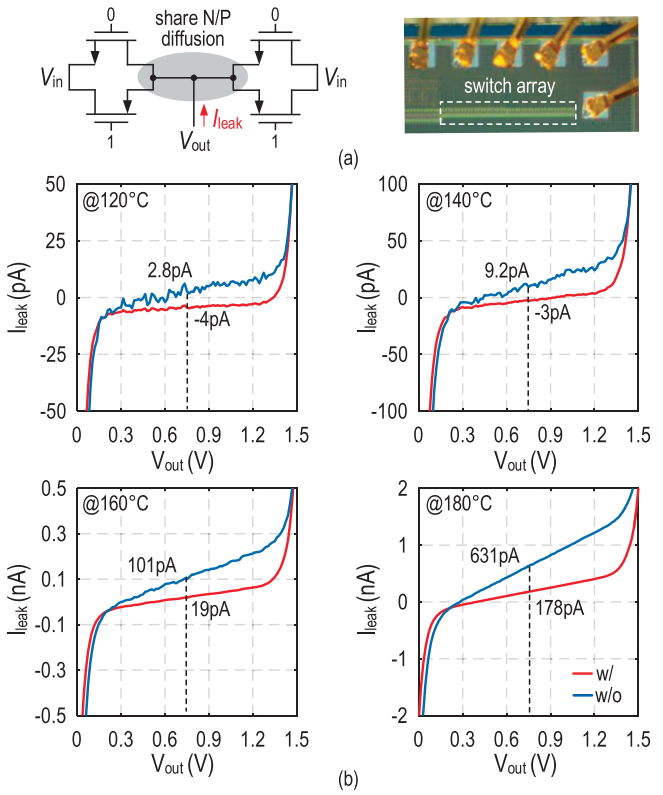


Fig. 12. (a) Leakage test structure of an analog multiplexer. (b) Measured I_{leak} at different temperatures (with and without body leakage compensation, V_{in} = 0.75 V).

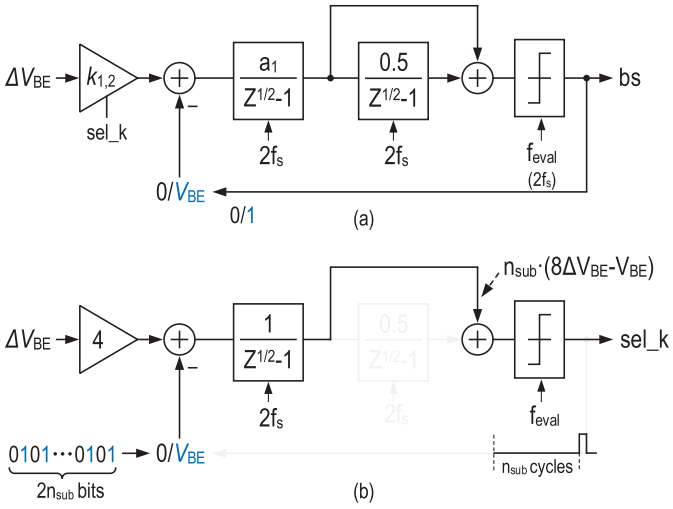


Fig. 13. (a) Double-sampled readout diagram during temperature conversion. (b) During the subrange decision.

its good tradeoff between quantization noise suppression, input range, and design complexity [23]. Fig. 13(a) shows its topology during temperature conversion. The gain for ΔV_{BE} is selected by *sel_k* at the beginning of each conversion. With a supply of 1.5 V, the first integrator gain α_1 is designed to be 1/3. Therefore, the maximum outputs of the two integrators are about $\pm 0.35 \cdot V_{BE}$, which can be satisfied by the designed current-reuse opamp. As the ADC input-referred noise from the integrator is $\propto (1 + 1/\alpha_1)^2$, it is not helpful to further reduce α_1. Effectively, the integrators and the quantizer operate at $2 \cdot f_s$, producing two *bs* output bits per clock cycle.

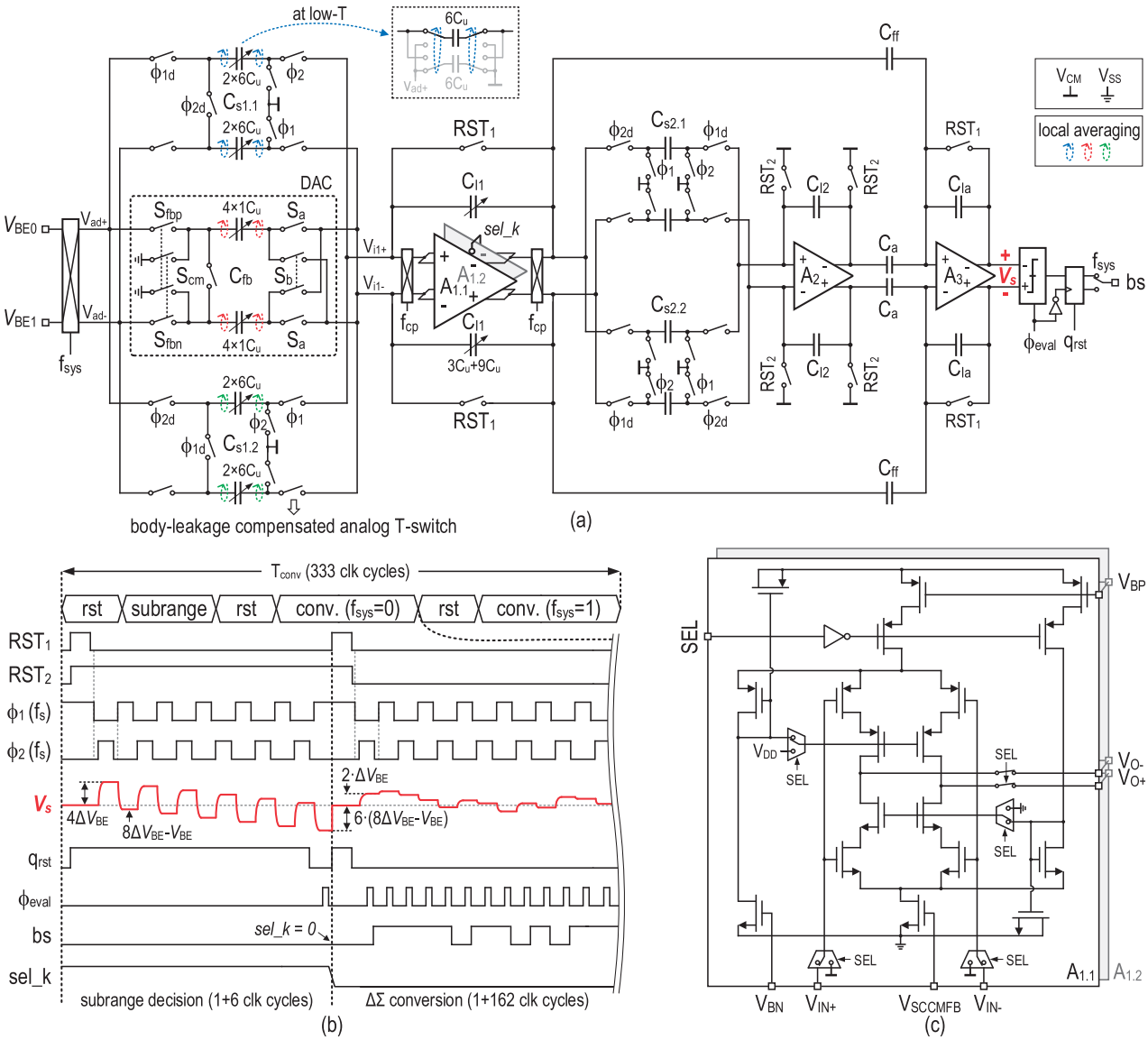


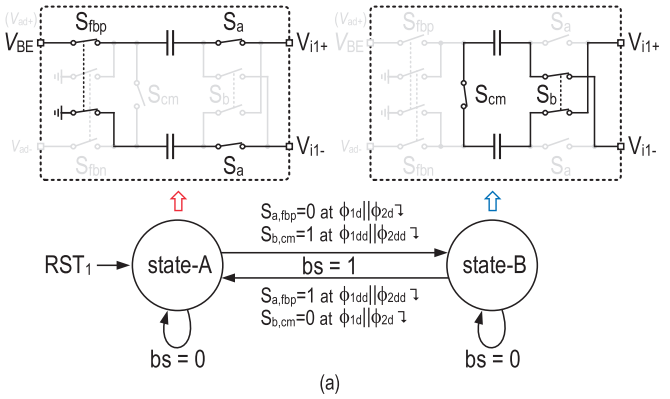
Fig. 14. (a) Double-sampled second-order ΔΣ modulator implementation. (b) Its simplified timing diagram (example with $f_{sys} = 0$ and in the low-T subrange). (c) Schematic of the two-slice opamp $A_{1.1,\,1.2}$.

Fig. 13(b) shows the ADC configuration during subrange decision. With the second integrator disabled, ΔV_{BE} is double-sampled with a gain of 4, and V_{BE} is sampled once per clock cycle. After running the ADC for n_{sub} clock cycles, the first integrator output is $n_{sub}\cdot(8\Delta V_{BE} - V_{BE})$, whose polarity is checked by the comparator to generate *sel_k* [see Fig. 5(d)]. In this work, we set $n_{sub} = 6$ to effectively suppress the variation of T_r induced by circuit noise and comparator offset.

2) Implementation and Operation: Fig. 14 presents the ADC schematic and its simplified timing diagram. It consists of two sampling paths $C_{s1.1}$ and $C_{s1.2}$, but with only one fully-floating feedback DAC C_{fb} to avoid quantization noise folding caused by DAC mismatch [25]. To implement $k_{1,\,2}$ and α_1, we configure $C_{s1.1,s1.2}/C_{fb}/C_{I1}$ to be $6C_u/1C_u/3C_u$ in the low-T subrange, and to be $12C_u/4C_u/12C_u$ in the high-T subrange, respectively. As shown in Fig. 5(b), the worst-case design targets are at −50 °C and 100 °C for the two subranges, respectively. In this work, the unit capacitance C_u is 260 fF to keep the total ADC input-referred noise from the frontend and readout below the target levels [30], [31].

Mismatch between $C_{s1.1,s1.2}$ and C_{fb} directly affects the accuracy of $k_{1,2}$. Applying the conventional DEM approach can result in a total of 336 switches for the 56 unit capacitors. As the k_1/k_2 ratio can be derived at RT, this design just performs a local averaging at the low-T subrange by involving all the unit capacitors of $C_{s1.1,s1.2,fb}$ within one temperature conversion. For example, as shown in Fig. 14(a), only $6C_u$ is used for ΔV_{BE} sampling at low-T. The other unused $6C_u$ is connected to V_{ad+} (to V_{ad-} for the other capacitor in the $C_{s1.1}$ pair) to reduce the frontend noise bandwidth. Their roles are exchanged periodically during conversion (i.e., at $f_s/36$). The same applies to $C_{s1.2}$. This can increase the effective capacitor area for matching, thus minimizing the spread of k_1 and the layout-dependent k_1/k_2 ratio error.

The local averaging of C_{fb} is *bs*-controlled to ensure its unit capacitors are equally involved for feedback. Specifically,



(a)

DAC state	state-A		state-B	
clk phase	ϕ_1 ϕ_2	ϕ_1 ϕ_2	ϕ_1 ϕ_2	ϕ_1 ϕ_2
S_a, S_{fbp}	1→0 at $\phi_{1d}\downarrow$	1→0 at $\phi_{2d}\downarrow$	0→1 at $\phi_{1dd}\downarrow$	0→1 at $\phi_{2dd}\downarrow$
S_b, S_{cm}	0→1 at $\phi_{1dd}\downarrow$	0→1 at $\phi_{2dd}\downarrow$	1→0 at $\phi_{1d}\downarrow$	1→0 at $\phi_{2d}\downarrow$

(b)

Fig. 15. (a) DAC state for $f_{sys} = 0$ (S_{fbn} is used instead of S_{fbp} for $f_{sys} = 1$). (b) Detailed switch control when $bs = 1$ ($S_{fbp,\,cm}$ are buffered version of $S_{a,\,b}$ in actual implementation to minimize signal-dependent switch charge injection, $\phi_{1d,1dd,2d,2dd}$ are the delayed and further delayed version of $\phi_{1,2}$, respectively, with $\phi_{1,2dd}$ and $\phi_{2,1dd}$ also being nonoverlapping signals).

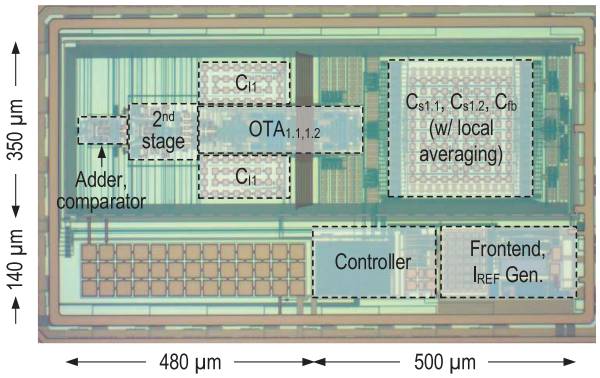


Fig. 16. Chip micrograph.

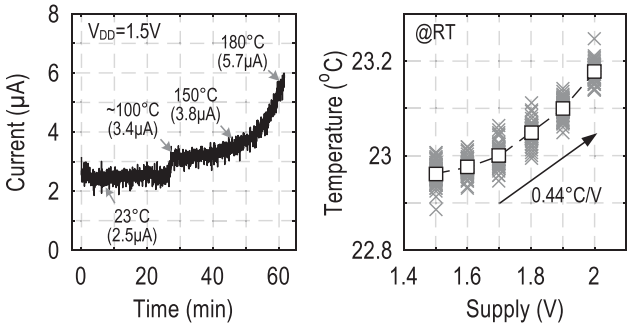


Fig. 17. Logged sensor current with increasing ambient temperature (left); and supply sensitivity at RT (right).

the positions of the four unit capacitors in the DAC are shifted once for every eight ones in *bs*. That is, its switching frequency depends on the density of "ones" in *bs*, which is temperature-dependent. As a result, this can introduce a frequency-varying noise tone to the output after intermodulation, especially with the chopping residue at $f_s/36$.

The first integrator consists of two ~80-dB dc-gain chopped current-reuse opamp slices $A_{1.1,1.2}$, as shown in Fig. 14(c), with only one enabled in each subrange. $A_{1.1,1.2}$ have different transistor sizing to maximize their respective output swing for the two subranges, while consuming 0.8 μA and 1.65 μA, respectively. Despite the reduced settling requirement, $A_{1.2}$ designed for the high-T subrange burns more power due to the 2× larger $C_{s1.1,s1.2}$ and degraded transistor g_m/I_d efficiency at high-T. The second integrator and summer, with much-relaxed gain, noise, and driving requirements, draw 170 nA each.

To avoid affecting the floating input $V_{i1+,\,i1-}$ of the first integrator (i.e., equal to the common-mode voltage $V_{DD}/2$ after reset), the varying common-mode voltages of V_{BE} and ΔV_{BE} are canceled by shorting the respective sampling plates of $C_{s1.1/s1.2/fb}$ during charge redistribution. Switches employed in the readout are analog T-switches with body leakage compensation to minimize both their channel and body leakages, thus minimizing their influence on $V_{BE0,\,1}$ during sampling [11], [14]. The use of low-leakage switches is also essential to minimize the drift of $V_{i1+,i1-}$ at high-T.

Fig. 15(a) depicts how a single DAC can achieve feedback at a speed of $2\cdot f_s$. After reset, it stays at state-A. When $bs = 1$, it switches to state-B, thus sampling $-V_{BE}$ for feedback. Next, if $bs = 0$, the DAC will stay at state-B, or switch back to state-A for feedback otherwise. The DAC control signals $S_{fbp/n,cm,a,b}$ are triggered by one of the falling edges of $\phi_{1d,1dd,2d,2dd}$ depending on the current DAC state and clock phase, as detailed in Fig. 15(b). For example, if the DAC is currently in state-B with the clock in ϕ_1, we can achieve feedback by turning off $S_{b,cm}$ at the falling edge of ϕ_{1d}, and then turning on $S_{a,fbp}$ at the falling edge of ϕ_{1dd}. Note that the DAC does not perform a "sampling" operation on V_{BE} when it switches from state-B to state-A. In this case, the noise in V_{BE} is not sampled by the first integrator, meaning that half of the feedback operations are free from the noise in V_{BE}. This is another advantage of employing a fully floating DAC in a double-sampled ADC.

In this design, one temperature conversion takes 333 clock cycles in total. System-level chopping, once per conversion via f_{sys}, can suppress the residual offset and $1/f$ noise by inverting the input polarity and averaging the decimated output.

IV. Experimental Results

Fabricated in a standard 0.18-μm CMOS process, the sensor prototype occupies an area of 0.42 mm^2. Fig. 16 shows the chip micrograph. The sinc^3 filter is implemented in FPGA for testing flexibility. However, it can be handily integrated on-chip. With a 1.5-V supply, the simulated average current of our customized sinc^3 filter is 55 nA running at the data rate of 80 kHz at RT. Clocked at 40 kHz, the sensor draws 2.5 μA at RT (230 nA from the digital controller), and 3.8 μA at 150 °C with a 1.5-V supply. As observed in Fig. 17, the sensor current further increases to 5.7 μA at 180 °C, with 2.08 μA consumed by the digital controller even after employing clock-gating and high-V_{th} devices. From 1.5 to 2 V, the measured dc supply sensitivity is 0.44 °C/V and 0.15 °C/V at RT and 180 °C, respectively, as limited by the reduced gain of the designed error amplifier in the frontend when supply voltage increases.

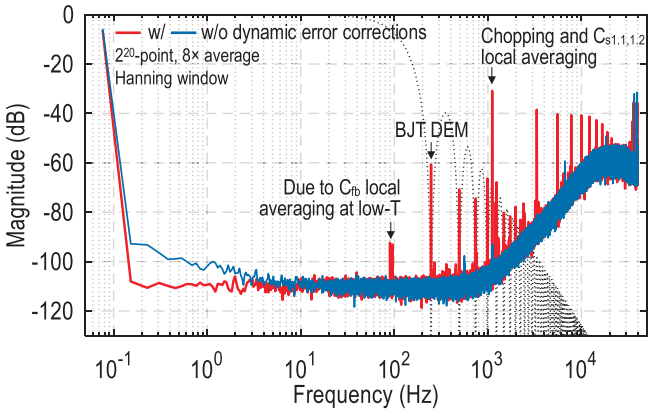


Fig. 18. Measured power spectrum of bs at RT, together with the sinc^3 filter response (dotted line) for its in-phase periodic switching noise suppression.

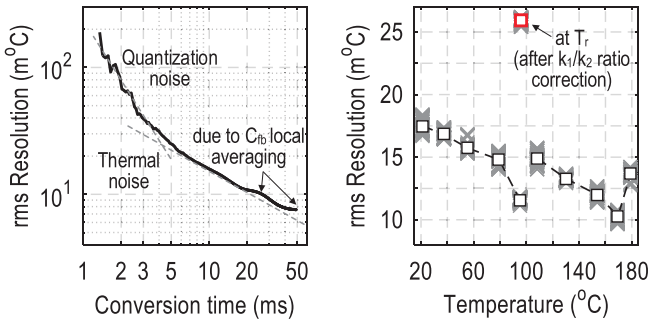


Fig. 19. Measured resolution over time (left); and sensor resolution at different temperatures above RT with a conversion time of 8.325 ms (right).

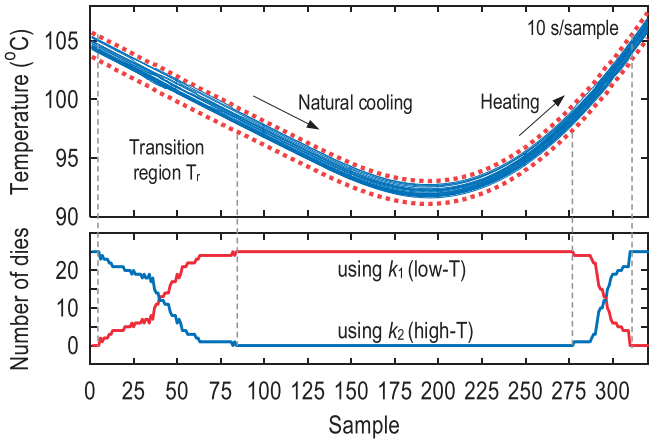


Fig. 20. Measured sensor output of 25 untrimmed dies around T_r to observe the subrange transitions.

Fig. 18 shows the measured power spectrum of the output bitstream at RT. Periodic noise tones caused by the dynamic error correction techniques are noticeable and can be suppressed by the digital filter. The noise tone introduced by the local capacitance averaging (active only in the low-T subrange) of C_{fb} is also visible, with its amplitude staying almost constant across temperature (frequency varies with temperature). The $1/f$ noise corner is suppressed to <150 mHz.

As shown in Fig. 19, with dynamic error correction enabled, the achieved kT/C-limited resolution is 17.6 m°C$_{\text{rms}}$ under a conversion time of 8.325 ms at RT, corresponding to a resolution-FoM of 9.7 pJ·K^2. The measured resolution at

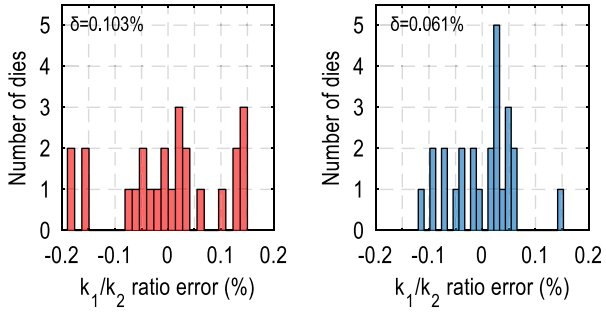


Fig. 21. Measured k_1/k_2 ratio error without (left) and with (right) capacitor local averaging. The conversion time is doubled for measuring the k_1/k_2 ratio.

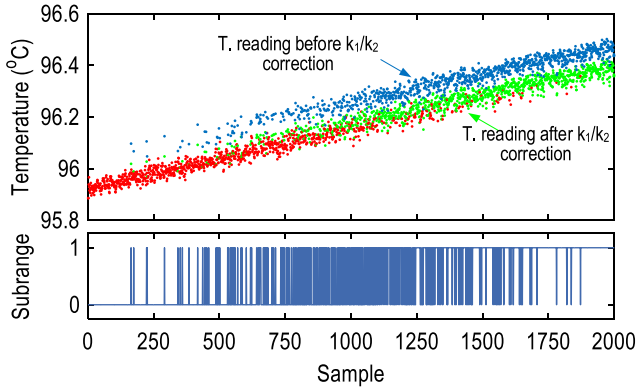


Fig. 22. Measured subrange transition of one typical die to illustrate the discontinuity at T_r between the two subranges.

150 °C and 180 °C is 12.3 m°C and 13.5 m°C, respectively. As a result, by exploiting a nonlinear readout with subranging, double sampling, and constant current biasing techniques, this work demonstrates a state-of-the-art resolution-FoM of 7.2 pJ·K^2 at 150 °C. The sensor resolution degrades to ~25 m°C at T_r mainly due to the residual step change after k_1/k_2 ratio error correction (see Fig. 22). Using a separate comparator with hysteresis for subrange decision can avoid this resolution loss, while at the cost of hardware and control overhead.

To investigate the subranging operation, we performed a slow temperature ramp test near T_r. Fig. 20 shows the measured responses from 25 untrimmed samples. The transition between $k_1 \leftrightarrow k_2$ is quite smooth. The transition temperatures, which lie between 96 °C and 105 °C (3σ), are also consistent during ramp up and ramp down.

We measure the k_1/k_2 ratio error for a batch of 25 samples at RT to perform gain calibration for the two subranges. As shown in Fig. 21, this error is 0.103% and 0.06% without and with local capacitance averaging, respectively. This gain accuracy is a result of using a relatively large capacitor, dedicated layout matching, and the application of the local averaging technique. Fig. 22 shows the measured discontinuity between the two subranges due to k_1/k_2 ratio error, which can be alleviated using k_1/k_2 ratio correction at RT (Section II-E).

To evaluate the sensor accuracy, we characterize these 25 samples from −50 °C to 180 °C in a climate chamber. After batch calibration, the constants required in (3) and (4) are derived to be $\alpha = 11.455$, $A = 650.23$, and $B = -286.63$.

TABLE I
PERFORMANCE SUMMARY AND BENCHMARK WITH STATE-OF-THE-ART CMOS TEMPERATURE SENSOR DESIGNS

	Up to 125 °C			**Extended sensing range**					
Reference	**[16]**	**[20]**	**[13]**	**[5]**	**[10]**	**[11]**	**This work**		
Sensor type	BJT	BJT	BJT	Resistor	BJT	BJT	**BJT**		
Technology (μm)	0.18 CMOS	0.16 CMOS	0.028 CMOS	0.18 CMOS	0.16 SOI	0.16 CMOS	**0.18 CMOS**		
Area (mm^2)	0.35	0.08	0.01	0.12	0.1	0.15	**0.42**		
Supply voltage (V)	1.6-2.2	1.5-2	1.8	1.8	1.6-2	1.8	**1.5-2**		
Sensing range (°C)	–40 to 125	–55 to 125	–25 to 125	–40 to 180	–55 to 200	–40 to 180	**–50 to 180**		
3σ inaccuracy (cal. points) (°C)	±0.25 (1) ±0.13 (1)[b]	±0.15 (vcal)[c]	±1.85 (0)	±0.4 (1)[d] ±0.11 (2)[d]	±0.4 (1)	±0.2 (1) ±0.25 (ha-vcal)[e]	**±0.45 (1)**		
Rel. inaccuracy (cal. points) (%)	0.3 (1) 0.16 (1)[b]	0.2 (vcal)[c]	2.47 (0)	0.36 (1)[d] 0.1 (2)[d]	0.31 (1)	0.18 (1) 0.23 (ha-vcal)[e]	**0.39 (1)**		
Conversion time (ms)	218	5.3	8.2	10	4.2	20	**8.3**		
Power at RT (μW)	9	5.1	18.8	52	35.2	9.8	**3.8**	**5.7**[f]	**8.5**[g]
Resolution (m°C)	1.67	20	150	0.46	20	23	**17.6**	**12.3**	**13.5**
R-FoM ($pJ{\cdot}K^2$)[a]	5.4	11	3500	0.1	59	103	**9.7**	**7.2**	**13**
Measured samples	25	19	76	20	7	24	**25**		

[a]Resolution FoM = Energy/Conversion × Resolution^2 [b]after 5th-order nonlinearity correction [c]voltage calibration
[d]with 6th-order nonlinearity correction [e]heater-assisted voltage calibration [f]at 150 °C [g]at 180 °C

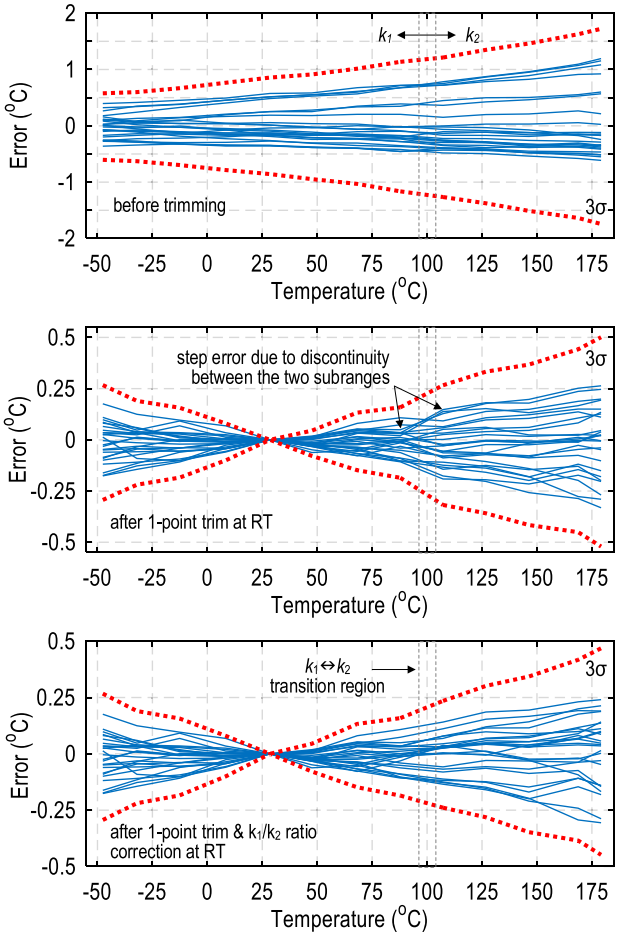


Fig. 23. Measured inaccuracy of 25 dies that are untrimmed (top); after 1-point trim (middle); and after further k_1/k_2 ratio error correction (bottom).

As observed in Fig. 23, the untrimmed inaccuracy is ±1.8 °C (3σ), which could be larger if more samples from different wafers are measured. With one-point trim at RT, the sensor inaccuracy is ±0.5 °C (3σ) as shown in Fig. 23 (middle). After the k_1/k_2 ratio correction, the achieved inaccuracy further improves to ±0.45 °C (3σ), ultimately limited by the absolute precision of k_1 and the residual spread of V_{BE}.

The designed sensor can operate at a measured temperature of up to ∼205 °C, mainly limited by the maximum stable input range of the second-order ΔΣ modulator. Considering the lifetime and robustness of bulk CMOS, we only characterize the sensor up to 180 °C. Table I benchmarks this work with state-of-the-art energy-efficient temperature sensors. This work achieves the lowest power consumption with a similar resolution at RT compared to [10], [11], and [20]. Among the designs with an extended sensing range, this work in bulk CMOS achieves a 6-to-10× higher energy efficiency than prior works [10], [11] with a comparable sensing range, resolution, and trimming effort (except for the resistor-based one [5]).

V. CONCLUSION

This article presents a low-power (3.8 μW at RT) BJT-based temperature sensor optimized for a wide sensing range from −50 °C to 180 °C. This sensor can achieve high full-range energy efficiency by exploiting subranging, double-sampling, constant current biasing, and nonlinear readout techniques, especially at high-T. Measurement results show a state-of-the-art resolution-FoM of 9.7 $pJ{\cdot}K^2$ at RT and 7.2 $pJ{\cdot}K^2$ at 150 °C. The switch body-leakage compensation scheme can maximally maintain the signal linearity at high-T, which enables a process-spread-limited sensing inaccuracy of ±0.45 °C (3σ) with 25 measured samples.

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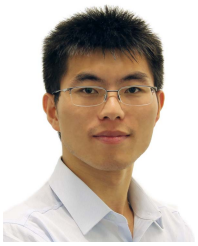

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